TERMINATION STRUCTURE FOR MOSGATED POWER DEVICES

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/394,038, filed July 3, 2003.

FIELD OF THE INVENTION

[0002] This invention relates to power MOSgated devices and more specifically relates to a novel trench termination for such devices

BACKGROUND OF THE INVENTION

[0003] Power MOSgated devices such as power MOSFETs and IGBTs are well known. Such devices may employ a planar or tench type active area but a termination structure is needed to terminate the active area. Such termination structures frequently employ spaced field rings and field plates. These require considerable area of the silicon die, particularly for high voltage devices, and increase the necessary die area. Generally, the termination size is about 3 to 5 times the required junction-receiving epitaxial silicon layer thickness, which increases as a function of blocking voltage capability. Thus, a planar termination requires space to "ramp down" the electric field from the edge of the active area to the device edge. The higher the device voltage is, the larger is the proportion of termination area to die area.

[0004] It would be very desirable to reduce the termination area without impacting the reliability of the termination.

BRIEF DESCRIPTION OF THE INVENTION

[0005] In accordance with the invention, a trench type bevel is formed at the edge of the active area or the edge of die, the top of the bevel extending downward from the outer periphery of the active area. The bevel may form a V groove bevel in the wafer at the die streets or within the die if the die contains plural active areas which are isolated from one another. Other bevels or trench structures can be used. The surface of the bevel or trench is coated with a thin layer of a high resistance but conductive film such as amorphous silicon which is used to electrically connect the drain and source of the device. As a high drain voltage is applied, in an N channel device for instance, a small leakage current flows through the linear amorphous silicon resistor so that the electrical potential distribution along the termination surface is linearly fixed. This linear voltage distribution along the amorphous silicon ensures that the surface electrical field is lower than the maximum field inside the active area. Thus, the active area will avalanche before the termination avalanches. With this structure, the termination size (width) can be dramatically reduced, typically, to a lateral distance about equal to the epi thickness, or even less. The novel termination also reduces device size overhead, especially for low current devices. The bevel angle can be adjusted to tradeoff the leakage current and termination size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a cross-section of a portion of a semiconductor MOSgated device which contains the termination structure of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0007] Referring to Figure 1, there is shown, in cross-section a typical planar power MOSFET 10 before singulation from its wafer at street 11. Any other MOSgated device could have been shown, such as an IGBT; and any topology could be used for the active area such as a trench or planar topology.

[0008] In the example of Figure 1, which is an N channel device (a P channel device could also be used with the invention), an N^+ silicon body or other substrate 12 is provided as usual, which conventionally receives a conductive drain electrode 13. An epitixially grown N^- layer 14 is conventionally grown atop substrate 12, for receiving the device junctions. The thickness and resistivity of the layer 14 is determined by the reverse voltage to be withstood by the device and are selected as well known. The active area in Figure 1 contains a well known structure of plural spaced P type base (or channel) diffusion stripes 15, 16 (which could be closed cells, or elements of a trench structure). The channel diffusions 15 and 16 contain conventional N^+ source regions 17 and 18 respectively. The invertible channels between the ends of the N^+ sources 17 and 18 and the ends of base regions 15 and 16 are covered by a conventional MOSgate structure comprising thin gate oxide layers 19, 20, 21 and polysilicon gate electrodes 22, 23 and 14 respectively. The polysilicon gate electrodes are then insulated as by LTO insulation oxide as usual, and a source electrode 30 is formed on the top surface of the active area.

[0009] In accordance with the invention, a bevel 40, which may be a vertical trench or V groove is formed in the silicon wafer, and is coated with a relatively high resistance coating or film 41 which will permit the flow of a small leakage current from drain 13 to source 30 when drain to source voltage is applied to the device. This resistive current path insures the control of the electric field along the length of the bevel 40 and insures that the device breakdown will occur within the active area silicon rather than at the periphery of the die. Preferably, the resistive coating or film 41 is amorphous silicon, but other materials can be used. Thus, Coating 41 can be formed of films including nitrides, oxides, and semi-insulating films like amorphous silicon, sipos, silicon-rich nitride, silicon carbide and the like; and combinations of such materials. Any suitable process can be employed to pattern the windows in these films after their formation and either before or after the fabrication of the MOSgated structure. Film 41 may have any desired, non-critical thickness.

[0010] The area required by the termination is drastically reduced, compared to prior planar terminations, and, for example, its lateral extent, labeled "TERMINATION" in Figure 1 can be less than the thickness of epitaxial region 14. By comparison, prior planar terminations have a lateral extend of 3 to 5 times the thickness of region 14.

[0011] The bevel angle can be varied as desired, depending on the device conditions, and can include a trench with vertical walls (at 90° to the upper surface of the wafer to any desired angle less than 90° to the upper surface. The coating 41 can have any desired thickness and conductivity, again depending on device conditions.

[0012] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.